REMARKS

Claims 1-16 are pending. Claims 13 has been canceled, and the subject matter thereof has been incorporated into claim 12. Reconsideration and withdrawal of the prior rejections are respectfully requested.

Claims 1 and 3 stand rejected under 35 U.S.C. § 112, 2 ¶, as being indefinite for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention.

Specifically, the Examiner has stated that claim 1 recites the limitation "control the first and second channels in dependance on said detection" in the 11th and 12th line of the claims. According to the Examiner, "this language is unclear and it appears applicant meant to state "control the first and second channels independently upon said detection."

With respect to this rejection, Applicant respectfully submits that the language referenced by the Examiner can mean that the first and second channels can be either independent or dependently controlled in dependence on detection. Accordingly, Applicant respectfully submits that the language of claim is definite. Therefore, reconsideration and .withdrawal of the rejection are respectfully requested.

The Examiner has stated that the claims 3 recites the limitation "controls the first and second channels each to simultaneously execute the single operation" in the 2nd and 3rd lines of the claim. According to the Examiner, "this limitation can mean both channels simultaneously execute

the same exact operation, i.e., using the same data, **or** each channel simultaneously executes the operation using separate data, i.e., the channels cooperate to perform the operation.

With respect to this rejection, Applicant respectfully submits that the limitation referred to by the Examiner means that both channels simultaneously execute the same operation. The "single operation", as set forth in claim 3, refers to a single data set. Therefore, Applicant respectfully submits that claim 3 is definite, and reconsideration and withdrawal of the rejection are requested.

Claims 12-13, 15, and 16 stand rejected under as anticipated by U.S. Patent No. 6,292,845 to *Fleck* et al., while claims 1, 2, and 5-7 have been rejected as unpatentable over the same reference in view of U.S. Patent No. 6,317,820 to *Shiell* et al. Claim 14 has been rejected as unpatentable over the *Fleck* et al. patent. Claim 3, 4 and 8-11 have been rejected as unpatentable over the *Fleck* et al. and *Shiell* et al. patents, and further in view of U.S. Patent No. 6,230,180 to *Mohamed* or U.S. Patent No. 5,365,476 to *Mukhanov*. These several rejection are traversed.

Rejections under 35 U.S.C. § 102(e)

According to the Examiner, U.S. Patent No. 6,292,845 to *Fleck* teaches a computer program product corresponding to the invention as currently claimed, including, *inter alia*, a set of identification bits, adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction.

Fleck, however, does not teach identification bits that cooperate with a decode unit for determining whether the instruction is a long or a dual operation instruction, as set forth in amended independent claim 12 and independent claim 16. Instead, the identification bits of *Fleck* cooperate with a type evaluation unit that controls the decision of the instructions through a multiplexer. A type evaluation unit does not have the same functionality as a decoder (i.e., the type evaluation unit does not decode). Accordingly, the rejection of claims 12 and 16 under 35 U.S.C. 102(e) should be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103(a)

Independent claim 1 is directed to a computer system comprising a decode unit that is operable to detect each instruction defining if the instructions is a single operation or two independent operations and to control two channels depending on the detection. *Fleck*, however, does not disclose or suggest a decoder with the functionality of controlling the channels or detect the type of the instructions, as set forth in independent claim 1. Instead, *Fleck* teaches a type evaluation unit that controls an alignment multiplexer. The alignment multiplexer of *Fleck* contains all the instructions retrieved from the memory and forwards them to a second multiplexer that selects the instructions according to their type into different type decoders, which receive only selected instructions. Due to this pre-decoding selection made by the multiplexer; there is no need to increase task-level parallelism. In other words, task-level parallelism exists in *Fleck* by way of the presence of a multiplexer.

Independent claim 15 describes a method of operating a computer system, where the instructions contain a set of designated bits at predetermined bit locations. The method performs the task of decoding and controlling each instruction. In *Fleck*, a type evaluation unit controls and evaluates the instructions through a multiplexer, in order to forward the information either to a load/store decoder or a integer decoder. As stated, a type evaluation unit does not have the same functionality as a decoder (i.e., the type evaluation unit does not decode). This would be readily understood by a person having an ordinary level of skill in the art

U.S Patent No. 6,317,820 to *Shiell* ("*Sheill*") discloses a long instruction word data processor including plural data registers, plural functional units and plural program counters and is selectively operable in either a first or second mode (see *Abs*). However this reference fails to cure the deficiencies of the *Fleck* et al patent. In addition, each processing channel in the claimed invention comprises a plurality of functional units. This feature, however, is also not found in *Fleck*, nor is it found in *Sheill*. Moreover, a person having the ordinary level of skill in the art would not have been motivated to modify *Fleck* by adding the task-level parallelism found in *Shiell* et al. because, as stated previously, task-level parallelism already exists in *Fleck*.

U.S Patent No. 5,365,476 to *Mukhanov* is directed to a three-port Josephson memory cell that has one input port (a data line) and two output ports (first and second sense lines). According to this reference, the memory cell receives a write enable pulse on a write line to store a bit of data from the data line as circulating supercurrent. The memory cell also receives a first read enable pulse on a first read line to enable assertion of the stored data onto the first sense line, and receives a second read enable pulse on a second read line to enable assertion of the stored data onto

the second sense line (see *Abs*). However, this reference also fails to cure the deficiencies of the *Fleck* et al patent. Specifically, this reference fails to disclose either a decoder that controls the channels or detects the type of the instructions, as set forth in independent claim 1.

U.S. Patent No. 6,230,180 to *Mohamed* is directed to multiply-accumulate units for use in digital signal processors. According to this reference, each multiply-accumulate unit includes a multiply unit which is coupled with two or more dedicated accumulators (see *Abs.*) However, this reference fails to cure the deficiencies of the *Fleck* et al. patent. Independent claim 8 recites a method that decodes an instruction to detect whether the instruction is a single, operation or two independent operations. When the instruction defines two independent operations, one in each channel, the operations are simultaneously executed, and when the instruction defines a single operation, the channels cooperate to implement a. single operation. *Mohamed*, however, teaches simultaneous execution of one single operation, and not of two independent operations within the functional units, as described in claim 8. Therefore, the simultaneous execution of dual operations is not taught by *Mohamed.*

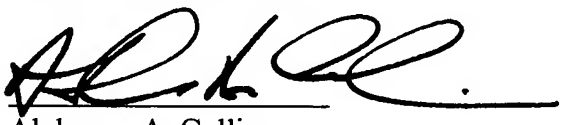
As previously discussed with regard to the rejection of claim 1, one having ordinary skill in the art would not have been motivated to replace the first and second processing channels of *Shiell* et al. with the processing channels of *Fleck.* Furthermore, it would not have been obvious to improve *Mohamed* in order to execute more independent operations simultaneously, because there is no need to increase task-level parallelism, as previously discussed. In view of the foregoing, applicant submits that all of the independent claims of the invention are patentable over the cited

prior art. Accordingly, reconsideration and withdrawal of all of the rejections are respectfully requested.

In light of the patentability of independent claims 1, 8, amended claim 12, 15 and 16, for the reasons above, dependent claims 3-7, 9-11 and 14 are patentable over the prior art.

In light of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this amendment, or the application in general, a telephone call to the undersigned would be appreciated since this expedite the prosecution of the application for all concerned.

Respectfully submitted,



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Docket No: 3598/0G117

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Sophie Wilson

Serial No.: 09/395,294 Art Unit: 2183

Confirmation No.: 5796

Filed: September 13, 1999 Examiner: Stephanie M. Deckter

For: AN INSTRUCTION SET FOR A COMPUTER

April 15, 2002

MARK-UP FOR AMENDMENT OF APRIL 15, 2002
PURSUANT TO 37 C.F.R. §1.121

IN THE SPECIFICATION:

On page 6, delete the second paragraph and insert the following new second paragraph:

Each register access path 12, 14 carries three addresses from the accessing unit, two source addresses SRC1, SRC2 and a destination address DST. In the case of data processing operations, the source addresses SRC1, SRC2 define registers in the register files 10,11 which hold source operands for processing by the data processing unit. The destination address DST

identifies a destination register into which a result of data processing will be placed. The operands and results are conveyed between the register file 10 or 11 and the respective data processing unit via the access paths 12, 14. In the case of load/store operations, the instruction formats allow memory access addresses A_x, A_y to be formulated from data values held in the registers as described in our copending application [(PWF Ref:)] (GB-9916566.4, entitled An Instruction Set for a Computer). The load/store units access a common address space in the form of a data memory 16 via a dual ported data cache DCACHE 15. For this purpose, each load/store unit has a 64 bit data bus Dx,Dy and a 64 bit address bus Ax,Ay.

IN THE CLAIMS:

12. (Amended) A computer program comprising

program code means which include a sequence of instructions all having the same predetermined bit length, said instructions including long instructions wherein said predetermined bit length defines two independent operations,

wherein the computer program product is adapted to run on a computer such that the long instructions control the resources of the computer in a first way, [and] the dual operation instructions control the resources of the computer in a second way, and each instruction includes a set fo identification bits locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction.

14. (Amended) A computer program according to claim [13] 12, wherein said designated bit locations in an instruction of n bits include at least the n/2th bit and nth bit.

Respectfully submitted,

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